Logic Circuits With High-Impedance Output State For Interconnection Of Ternary And Binary CMOS Digital Circuits And Systems

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Abstract – Possibilities and principles for interconnection of CMOS ternary circuits and systems with binary common buses in digital circuits and systems are considered and described in the paper. Proposed are circuits with high-impedance output state for interconnection that perform signal conversion from ternary to binary CMOS digital system. General structure and general principle for design of such circuits are shown and described first. Then, the concrete circuit solutions are proposed and described. The circuits with one ternary input and the circuits with any number of ternary inputs are given and described. All proposed circuits were analyzed by computer simulations. All considerations, descriptions and conclusions were confirmed by simulation.

Key words: CMOS logic circuits and systems, Ternary circuits, Binary circuits, Interconnection circuits, High-impedance output state

I. INTRODUCTION

The binary digital systems and circuits are still dominantly used in practical applications. Possibilities and interest for implementation of so-called multiple-valued or MV digital systems and circuits are increased with development of VLSI technologies [1-3]. The greatest interest exists for ternary and quaternary MV circuits and systems [1-5]. The first developed and practically implemented have been ternary MV circuits and systems. Later, the greatest practical interest exists for research and application of quaternary logic systems and circuits.

The main reasons that the binary systems are mainly used are great investments into research, development, design and production of binary systems [1-5]. Great investments into realization of binary peripheral devices that consequently will be still very long period in use are also very important. So, there is a practical interest for development, implementation and application of so-called mixed digital systems [1,2,3].

Mixed MV systems use combination of binary logic circuits and MV logic circuits. One part of the system is realized using MV logic circuits and other part of the system is realized using binary logic circuits. MV logic circuits are also very often used for implementation of some functions inside binary digital system [1-3].

In the mixed MV systems it is needed to perform conversion of digital signals from binary form into appropriate MV form, and vice versa. Appropriate logic circuits for interconnection and conversion have to be used at places where is performed interconnection of binary parts and MV parts of the system [1,2].

The common buses are very often used methods for interconnection of functional units and circuits and for data transmission in the binary and mixed MV digital systems [1,2]. Connection to the common buses is implemented by the logic circuits with high-impedance output state. Due to the same reasons as in the binary systems, the common buses and the logic circuits with high-impedance output state are also used in ternary and mixed digital systems.

The advantages and reasons for application of the CMOS technology in implementation of binary digital systems and circuits are very well known. So, there is interest to develop and use CMOS ternary and mixed MV circuits and systems. All these good characteristics of CMOS technology should be also kept in the ternary and mixed logic systems and circuits.

Principles for implementation of CMOS logic circuits with high-impedance output state for conversion of ternary digital signals into binary digital signals are considered and described in the paper. The circuits are used for interconnection of ternary CMOS circuits and systems with binary common buses.

II. GENERAL STRUCTURE AND PRINCIPLE FOR CIRCUITS DESIGN

General structure and principle for design of logic circuits with high-impedance output state for interconnection of ternary and binary CMOS digital circuits and systems are shown in Fig.1.

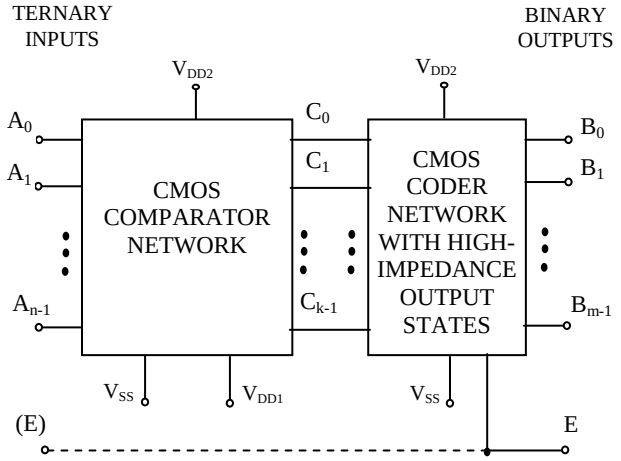

Fig.1. Structure and principle for realization of CMOS logic circuits for interconnection.

The shown structure consists of CMOS comparator network at the inputs and CMOS coder network with high-impedance output states at the outputs. There are *n* information ternary input logic signals and *m* binary output signals in the given structure. Also, there is one binary control input signal E for control of circuit output states. The CMOS comparator network is supplied by three supply voltages corresponding to ternary logic states and levels: V_{SS} (logic 0), V_{DD1} (logic 1) and V_{DD2} (logic 2). The output CMOS coder network is supplied by two supply voltages corresponding to binary states and levels: V_{SS} (logic 0) and V_{DD2} (logic 1). For one logic state (logic state 2) at the control input E the outputs of the circuit are enabled and the circuit operates as the standard CMOS logic circuit for ternary to binary signal conversion. For other logic state (logic state 0) at the control input E output CMOS transistors are turned off and the circuit outputs are in the high-impedance state. The control of circuit outputs can be performed from ternary signals side or from binary signals side.

A. *CMOS Comparator Network*

Ternary logic signals A_i are applied at the inputs of the comparator network. The binary logic signals C_i are obtained at the outputs. The network compares input ternary signals A_i with corresponding voltage thresholds and generates control signals C_i for CMOS coder network. Number of comparator network outputs depends on number of input ternary signals and number of output binary signals. Since here are used ternary input signals there are two voltage thresholds for comparison at any ternary input. The voltage thresholds are voltage values corresponding to the middle level between ternary logic levels:

$$V_{T1} = \frac{V_{SS} + V_{DD1}}{2}, \quad (1)$$

$$V_{T2} = \frac{V_{DD1} + V_{DD2}}{2}. \quad (2)$$

The lower voltage threshold is marked with V_{T1} and the higher voltage threshold is marked with V_{T2}. CMOS comparator network consists of CMOS voltage comparators at every input. There are more known solutions of CMOS voltage comparators.

B. CMOS Coder Network With High-Impedance Output States

The CMOS coder network with high-impedance output states is binary logic network. The task of the network is to generate output binary signals B_i depending of states at ternary inputs A_i and state at control input E. The network generates output binary signals B_i in accordance with state of binary signals C_i at the outputs of CMOS comparator network and state of control signal E. It can be designed and realized in the same way as standard CMOS coder networks and standard CMOS circuits with high-impedance output state.

III. PROPOSED INTERCONNECTION CIRCUITS

It can be designed and implemented more concrete solutions of such CMOS logic circuits for ternary to binary interconnection based on the shown and described structure from Fig.1.

A. *Circuits with one ternary input*

General scheme of circuit with one ternary input is shown in Fig.2. The circuit has two binary outputs (B_0 and B_1), one ternary information input (A) and one binary control input E. Two voltage comparator circuits (comparator 1 and comparator 2) are used at the input to compare input ternary signal A with voltage thresholds V_{T1} and V_{T2}. At the comparator outputs are generated binary signals C_0 and C_1. This signals are connected to the CMOS coder network with high-impedance output states that generates needed output binary signals. For every possible state at the ternary input A and binary input E it is obtained appropriate state at binary outputs B_0 and B_1.

CMOS Comparator Circuits

As the voltage comparator circuits (comparator 1 and comparator 2) can be used different known CMOS comparator solutions. That solutions have disadvantages in existing of static energy consumption and in need to generate referent voltages (comparison voltage thresholds

V_{T1} and V_{T2}). Here are proposed and shown solutions without such disadvantages, without static energy consumption and without need to generate comparison voltage thresholds V_{T1} and V_{T2}. Also, there is voltage histeresys in transfer characteristic and increased noise immunity in the circuits. The circuits perform voltage comparison and voltage level shifting at the output. The circuits are based on principles described in paper [6].

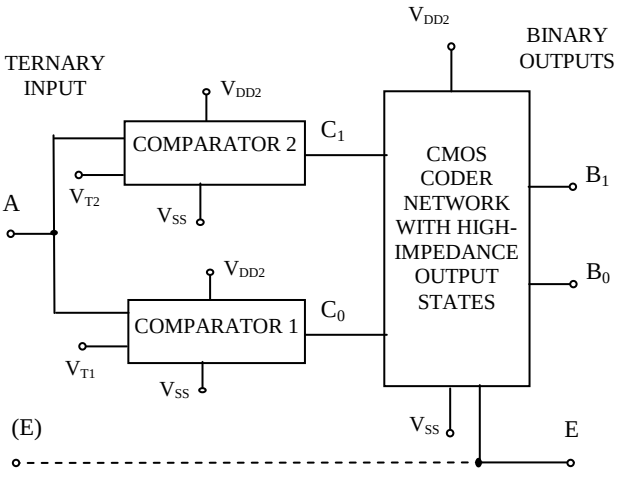

Fig.2. Circuit with one ternary input.

Proposed schemes of CMOS voltage comparators are shown in Fig.3. Comparator for comparison with lower voltage threshold V_{T1} (comparator 1) is shown in Fig.3a. Comparator for comparison with higher voltage threshold V_{T2} (comparator 2) is shown in Fig.3b.

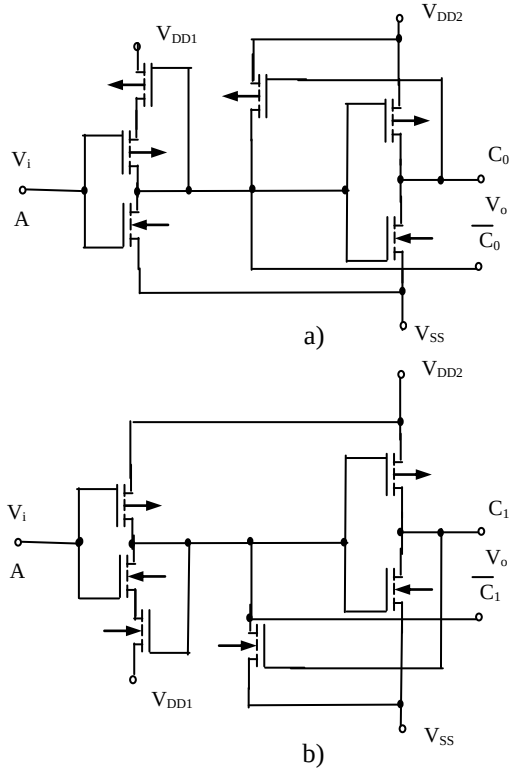

Fig.3. Proposed CMOS voltage comparators.

Operation of proposed CMOS voltage comparators was analyzed by PSpice simulations. Static voltage transfer characteristics of the voltage comparators are shown in Fig.4. By solid line is shown characteristic for comparator 1 (Fig.3a) and by dashed line is shown characteristic of comparator 2 (Fig.3b). In simulations were used technology parameters of one CMOS process [7] and supply voltages V_{SS}=0V, V_{DD1}=5V, V_{DD2}=10V. It can be seen that this circuits have histeresys in transfer characteristic and increased noise immunity. Value of voltage thresholds and voltage histeresys depend on supply voltages V_{SS}, V_{DD1}, V_{DD2} and on used CMOS transistors characteristics. It can be seen that the threshold voltage of the comparator 1 is approximately equal to V_{T1} and the threshold voltage of the comparator 2 is approximately equal to V_{T2}, that are given by equations (1) and (2).

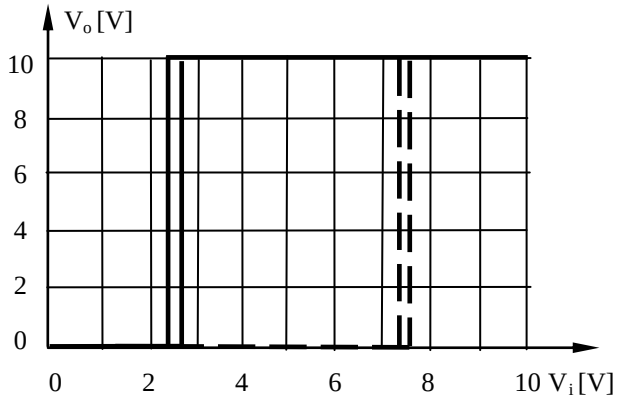

Fig.4. Static voltage transfer characteristics of proposed CMOS voltage comparator circuits.

Dynamic characteristics of proposed comparator circuits were also analyzed. Average delay time t_{da} of proposed circuits as a function of capacitive load C_L is shown in Fig.5. Average delay times of both circuits are approximately equal. The given results were obtained by PSpice simulations for the same conditions as for static transfer characteristics simulations.

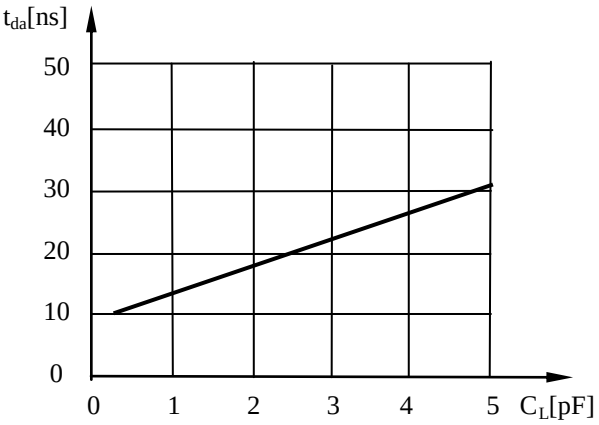

Fig.5. Average delay time of proposed CMOS voltage comparators as a function of capacitive load.

CMOS Coder Network With High-Impedance Output States

The CMOS coder network with high-impedance output states generates needed output binary signals B_0 and B_1 based on binary signals C_0 and C_1 and binary signal E. When is E=0 (voltage V_{SS}) the circuit outputs are disabled and in the high-impedance states. For E=2 (voltage V_{DD2}) binary outputs are enabled and output binary states depend on state at binary signals C_0 and C_1. It can be shown that for E=2 the output signals as a function of the input signals of the coder network are given by:

$$B_0 = \overline{C_1} \cdot C_0 = \overline{C_1 + \overline{C_0}}, \quad (3)$$

$$B_1 = C_1. \quad (4)$$

Since given voltage comparator circuits (Fig.3) have both outputs, noninverting and inverting output, for implementation of the CMOS coder network can be used both outputs to obtain simpler CMOS coder network.

The CMOS coder network has high-impedance output states. So, for implementation of the coder network can be used CMOS logic circuits with high-impedance output states (so called three-state CMOS circuits). The simplest method for implementation of coder network is to use CMOS three-state circuits at the outputs of coder network realized by standard CMOS logic circuits using equations (3) and (4). There are more ways to implement CMOS three-state circuits [8]. But, here is proposed other way to implement coder network that uses smaller number of CMOS transistors and has improved characteristics. It is based on integration of three-state logic into standard CMOS logic circuits. Here are proposed two such possible implementations.

Simple implementation of CMOS coder network with high-impedance output states is shown in Fig.6. It uses smaller number of CMOS transistors, but has greater delay times for greater capacitive loads.

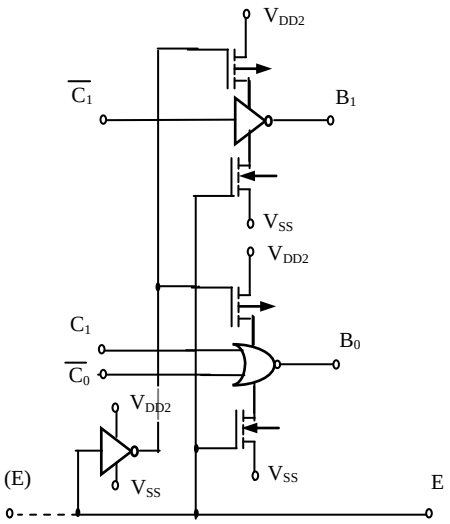

Fig.6. Simple CMOS decoder network with high-impedance output states.

Improved implementation of CMOS coder network with high-impedance output states is shown in Fig.7. The circuit uses greater number of CMOS transistors, but has smaller delay times for greater capacitive loads.

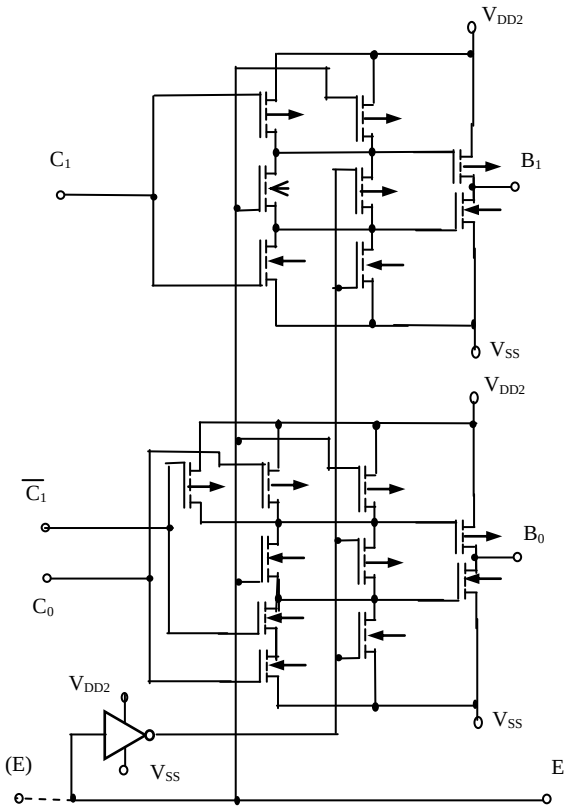

Fig.7. Improved CMOS decoder network with high-impedance output states

Circuit Simulation Results

The complete CMOS circuit with high-impedance output state and one ternary input for interconnection of ternary and binary circuits and systems was designed on the basis of described principles and given circuits. The circuit was analyzed by simulations. The output signals as a function of input signal changes when the outputs are enabled (E=2) obtained by PSpice simulation are shown in Fig.8. In the simulations were used the same technology parameters and the same supply voltages as in previous simulations. At the ternary input was applied slow changing signal that enables obtaining of all possible binary states at the outputs of the circuit, what can be seen in Fig.8. That is confirmation of proper operation of the circuit. Input ternary signal was marked by V_i, signal at binary output B_0 was marked by V_{o0} and signal at binary output B_1 was marked by V_{o1}.

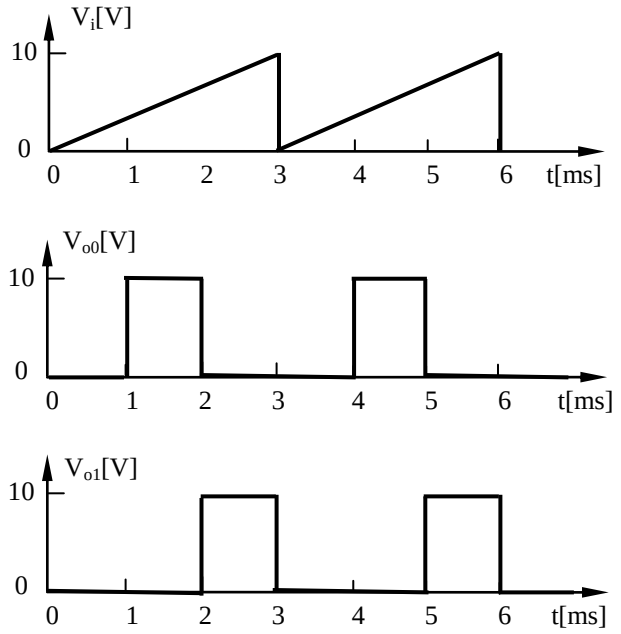

Fig.8. Output signals as a function of input signal changes when outputs are enabled for circuit with one ternary input.

B. Circuits With More Ternary Inputs

General structure and principle for implementation of circuits with more ternary inputs (with any number of ternary inputs) is shown in Fig.1. Implementation of concrete circuit includes determination of number of ternary inputs and number of binary outputs, design of input CMOS comparator network and design of output CMOS coder network with high-impedance output states.

Input CMOS comparator network can be implemented using same described voltage comparators from Fig.3. Two such comparators need to be used at every circuit input, according to principle from Fig.2.

Output CMOS coder network with high-impedance output states can be implemented according to same principles as for circuit with one ternary input. Based on binary signals from outputs of comparators and binary control signal E the network generates output binary signals

As an example of proposed and described principle, the proposed general scheme for implementation of circuit with two ternary inputs and four binary outputs is shown in Fig.9. At every of ternary inputs in Fig.9 are used two CMOS voltage comparators shown in Fig3.

CMOS output coder network with high-impedance output states generates output binary signals B_i on the basis of binary signals C_i from voltage comparators outputs and binary enable signal E. For E=0 the output binary signals B_i are disabled and in high-impedance state. When is E=2 the binary outputs B_i are enabled. Than, it can be shown that for circuit from Fig.9 with two ternary inputs the output signals for coder network are given by:

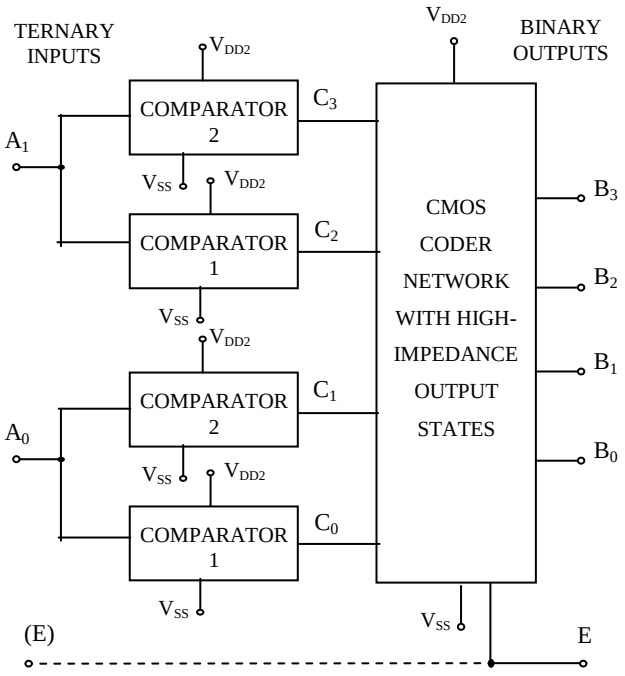

Fig.9. General scheme of circuit with two ternary inputs and four binary outputs.

$$B_0 = \overline{C_2}\cdot\overline{C_1}\cdot C_0 + \overline{C_3}\cdot C_2\cdot\overline{C_0} + \overline{C_3}\cdot C_2\cdot C_1 + C_3\cdot\overline{C_1}\cdot C_0, \quad (5)$$

$$B_1 = \overline{C_2}\cdot C_1 + C_2\cdot\overline{C_0} + C_3\cdot\overline{C_1}, \quad (6)$$

$$B_2 = \overline{C_3}\cdot C_2\cdot C_0 + C_3\cdot\overline{C_1}, \quad (7)$$

$$B_3 = C_3\cdot C_1. \quad (8)$$

As for circuit with one ternary input, for implementation of the coder network can be used CMOS logic circuits with high-impedance output states (so called three-state CMOS circuits). The simplest method is to use CMOS three-state circuits at the outputs of coder network realized by standard CMOS logic circuits using equations (5) to (8). Here is also used way to implement coder network that uses smaller number of CMOS transistors, has improved characteristics and is based on integration of three-state logic into standard CMOS logic circuits.

On the basis of proposed and described solutions it was designed complete scheme and circuit with two ternary inputs and four binary outputs. The circuit was in details analyzed using PSpice simulations. The simulations have confirmed proper operation of the circuit and all previous descriptions and considerations.

Described principles and scheme from Fig.9 enable to obtain such CMOS circuit for interconnection of ternary and binary digital circuits and systems with any number of ternary inputs and any number of binary outputs. Using concrete proposed solutions of CMOS comparators (Fig.3) and proposed way of comparators

application, as well as proposed ways for obtaining output CMOS coder circuit with high-impedance output states it is possible to obtain concrete schemes of such interconnection circuits with needed number of inputs and outputs.

IV. CONCLUSION

Very well known advantages of MV digital systems and great investments and experience in research, implementation, design and application of binary digital systems are the main reasons for increased interest for usage of mixed digital systems. Practically great interest exists for mixed MV systems where are used ternary and binary parts of the system. That requires practical application and usage of appropriate logic circuits for interconnection of ternary and binary parts of digital systems.

General structure and principles of implementation and design of CMOS circuits with high-impedance output states for interconnection of ternary and binary CMOS digital circuits and systems using common buses that are proposed in the paper are clear and relatively simple. Obtained circuits for interconnection are logic circuits without static power consumption (if we neglect MOS transistors leakage currents). Also, it is not needed to generate two referent voltages for comparison, but characteristics of standard CMOS inverters are used. It was achieved using proposed CMOS voltage comparators. Two proposed ways for design of CMOS coder network with high-impedance output states give possibility to implement circuits adopted to concrete working conditions at the place of circuit application. The circuits obtained using simple CMOS coder network, comparing with circuits using improved coder network, use less number of transistors. But, such circuits have greater propagation delay times for greater capacitive loads. The circuits obtained using improved CMOS coder network, comparing with circuits using simple coder network, use greater number of transistors. But, such circuits have smaller propagation delay times for greater capacitive loads.

Principles and elements used in realization of circuits with one ternary input are also used in realization of circuits with more ternary inputs (with any number of ternary inputs). The same pair of voltage comparators is used for every new ternary input. Output coder network with high-impedance output states is implemented on same principle as for circuits with one ternary input, but is more complex and has more inputs and outputs.

Proposed and described circuits are suitable for interconnection of ternary and binary circuits and subsystems inside of CMOS VLSI monolithic integrated circuits. Also, the circuits can be used as output circuits of monolithic CMOS integrated circuits or as separate CMOS integrated circuits for interconnection with smaller scale of integration.

To be possible to compare results of simulations and analysis with earlier obtained results for some other circuits in simulations were used parameters of one older CMOS technology process.

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